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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,645	05/09/2006	Patrice Gamand	FR 030143	1784

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EXAMINER	
MALEK, MALIHEH	
ART UNIT	PAPER NUMBER
2813	

NOTIFICATION DATE	DELIVERY MODE
07/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/578,645	GAMAND, PATRICE	
	Examiner	Art Unit	
	MALIHEH MALEK	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the application filed on 05/09/2006.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (Pub. No.: US 2004/0164371 A1) in view of O'Brien et al. (Pub. No.: US 2004/0048410 A1), herein O'Brien.

Regarding claim 1, Kang teaches a method of manufacturing a resonator within a semiconductor device (abstract), said semiconductor device comprising a substrate (Z_HO) with a first (XX') and a second (YY') axes which are perpendicular (substrate 100, [0018] and Fig.1A), wherein said method comprises the steps of: etching a hole (TR) in the substrate (Z_HO) ([0019], *Kang teaches forming a trench by an oxide layer applied to the silicon substrate 100 and etched according to a predefined mask. The predefined mask allows removal of oxide in order to create insulating mounts 106 for the mounting of a beam*) creating a first doping zone (Z_DIFF1) inside and around the hole (TR) for defining a first electrode, partitioning said first electrode into two electrodes (ELEC1, ELEC2) (104/105 and substrate, [0018]), applying a delimited oxide deposit (Z_OXI) inside and around the hole (TR) according to a specific deposit pattern (M_ONO) (110, [0020]-[0021], *Kang teaches the sacrificial layer 110 to be any material that can be removed without removing other material*), defining a second doping zone (Z_DIFF2) fully covering the hole (TR) (120, [0022]), removing the oxide deposit (Z_OXI) ([0023]) in order to define an element forming the resonator capable of vibrating between the two electrodes (ELEC1, ELEC2), wherein the partition of the two electrodes (ELEC1, ELEC2) is obtained by implanting a first dopant through a partitioning pattern. (M_ARBOR) ([0018]).

However, regarding claim 1, Kang does not specifically teach a second doping zone (Z_DIFF2) as the material covering the hole (TR).

In the same field of endeavor, regarding claim 1, O'Brien teaches a method for creating a MEMS structure comprising a second doping zone 156 as the material covering the hole to increase the conductivity ([0045] and Figs. 31-36). O'Brien also teaches an oxide sacrificial layer 147 ([0046]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Kang by incorporating the second doping zone of O'Brien to increase the conductivity (O'Brien, [0045]).

Regarding claim 2, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein the implant (AR) partly covers the hole (TR) at its bottom and sides as well as the substrate surface adjoining said hole (TR) ([0018], Kang teaches the implant that partly covers the hole (TR) at its bottom. Having implantation on the sides as well as the substrate surface adjoining the hole seems to be a matter of higher convenience).

Regarding claim 3, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein the first dopant is Argon or Boron ([0018]).

Regarding claim 4, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein said hole (TR) is a trench or a pore which is substantially perpendicular to the substrate surface (Z_HO) ([0019]). Kang teaches *forming a trench by an oxide layer applied to the silicon substrate 100 and etched according to a predefined mask. The predefined mask allows removal of oxide in order to create insulating mounts 106 for the mounting of a*

beam, therefore it would have been obvious to form a trench in the substrate compare to the forming trench by forming oxide mounts.

Regarding claim 5, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein the substrate (Z_HO) is of a high-ohmic type and the first doping zone (Z_DIFF1) is of a low-ohmic type. Kang teaches doping the substrate 100 which is same as the first doping zone (Z_DIFF1). It is well-known in the art that the doped zone is a low-ohmic type. Therefore, it would have been obvious to one having ordinary skill in the art to provide a doping zone on the substrate which is a lower-ohmic type.

Regarding claim 6, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein the specific deposit pattern (M_ONO) extends along the second axis (YY'), the inside of said deposit pattern (M_ONO) allowing the oxide to be settled inside the entire hole (TR) and at the substrate surface adjoining said hole (TR) and beyond (Figs. 4D-E).

Regarding claim 7, O'Brien teaches a method of manufacturing a resonator within a semiconductor device wherein the second doping zone (Z_DIFF2) is obtained by means of a second doping pattern (NIPS) extending along the first axis (XX') of the semiconductor (SI), the inside of said pattern (M_PS) allowing a second dopant to be settled totally inside the hole (TR) (Figs. 31-36).

Regarding claim 8, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein the inside of said pattern (M_PS) permits a second dopant to cover totally the oxide deposit adjoining the hole (TR) and beyond (Fig. 4E-F).

Regarding claim 9, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein said method comprises a further step of adding first pads (CTA) along the second axis (YY') on each side of the hole (TR), said pads being in contact with the first doping zone (Z_DIFF1) (Fig. 5 and [0024], *The H-beam 208 includes four mounting pads 212a-c/b-d and that mount to insulating pads that attach to a silicon substrate 214*).

Regarding claim 10, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein said method comprises a further step of adding second pads (CTA) along the first axis (XX') on each side of the hole (TR), said pads being in contact with the second doping zone (Z_DIFF2) (Fig. 5 and [0024], *The H-beam 208 includes four mounting pads 212a-b/c-d and that mount to insulating pads that attach to a silicon substrate 214*).

Regarding claim 11, Kang teaches a method of manufacturing a resonator within a semiconductor device wherein said semiconductor device comprises a substrate (Z_HO) with a first definition zone (Z_HL) where the resonator is built (Fig. 5).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Blanchard (Pat. No.: US 6,812,056 B2) teaches a single crystal semiconductor region fabricated in a semiconductor wafer. The region is either cantilevered, supported at one or both ends, or midpoint, or supported at multiple locations. After a pattern and etch step, a dielectric fill step is performed to define the boundaries of the region in the semiconductor wafer. Oxygen or nitrogen is implanted in the semiconductor wafer on a surface area of the semiconductor wafer that corresponds to a top surface of the region.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MALIHEH MALEK whose telephone number is (571)270-1874. The examiner can normally be reached on Mon-Fri, 8:30-6pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 3, 2008

/M. M./
Examiner, Art Unit 2813

/Jack Chen/
Primary Examiner, Art Unit 2813